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FOR

ELECTROSTATIC DISCHARGE PROTECTION FOR A MIXED-VOLTAGE DEVICE USING A STACKED-TRANSISTOR-TRIGGERED SILICON CONTROLLED RECTIFIER

BY

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DESCRIPTION OF THE INVENTION

Field of the Invention

[001] This invention pertains in general to a semiconductor device, and, more particularly, to an electrostatic discharge protection circuit using a stacked-transistor-triggered rectifier device.

Background of the Invention

[002] A semiconductor integrated circuit (IC) is generally susceptible to an electrostatic discharge (ESD) event that may damage or destroy the IC. An ESD event refers to a phenomenon of electrical discharge of a current (positive or negative) for a short duration in which a large amount of current is discharged through the IC. Protecting an IC from an ESD event, therefore, is an important factor to be considered in IC design. In deep sub-micron, or small geometry, complementary metal oxide silicon (CMOS) technology, the protection of an IC becomes an even more important issue due to the implementation of thin oxide layers in such ICs. As oxide layers become thinner, the voltage margin between oxide breakdown voltage and drain snapback breakdown voltage of a metal-oxide-silicon ("MOS") transistor is reduced.

[003] It also follows that transistors having a smaller geometry operate in different voltage levels than transistors with a larger geometry, and the transistors with a smaller geometry cannot withstand an ESD level tolerable to transistors with a larger geometry. As designers continue to design ICs with increasingly smaller geometries, it is inevitable that ICs having transistors with different geometries will

be interconnected for a variety of applications. Therefore, with a mix of different operating voltage levels, input/output (I/O) pads of mixed voltage ICs must be designed to avoid electrical overstress and prevent undesirable current leakage paths. An ESD protection circuit must also satisfy the same I/O interface conditions and constraints, and be able to be triggered so as to prevent the internal circuitry from being damaged. Many schemes have been implemented to protect a mixed voltage IC from an ESD event.

[004] Fig. 1 is a reproduction of Fig. 2 of U.S. Patent No. 5,932,918 to *Krakauer*. *Krakauer* describes an ESD protection circuit for mixed voltage I/O circuits. Fig. 1 shows an ESD protection device using two n-type MOS (NMOS) transistors stacked in a cascade configuration at the I/O buffer to protect a mixed voltage IC. The two stacked-NMOS transistors have common nodes formed by a shared diffusion. However, due to the reduced gate oxide breakdown voltage in a mixed I/O application, the MOS gate oxide of the I/O buffer might be damaged under an ESD event before the lateral NPN bipolar transistor in the stacked NMOS transistors can be turned on to divert the ESD current away from the internal circuits.

[005] It is accordingly a primary object of the invention to provide an electrostatic discharge protection circuit using a stacked-transistor-triggered silicon controlled rectifier device that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

SUMMARY OF THE INVENTION

[006] In accordance with the invention, there is provided an electrostatic discharge protection circuit that includes a rectifier, having an anode and a cathode,

including a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, and a second n-type portion contiguous with the second p-type portion, wherein the first p-type portion is coupled to the anode and the second n-type portion is coupled to the cathode, a first transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the first n-type portion of the rectifier, a second transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the second terminal of the first transistor, and the second terminal is coupled to the second n-type portion of the rectifier, and a voltage coupling circuit having a first terminal, a second terminal, a third terminal, and a fourth terminal, wherein the first terminal is coupled to the anode of the rectifier, the second and the third terminals are respectively coupled to the gate terminals of the first and second transistors, and the fourth terminal is coupled to the cathode.

[007] In one aspect, the voltage coupling circuit provides a first voltage signal to the gate of the first transistor and a second voltage signal to the gate of the second transistor to turn on the rectifier.

[008] In another aspect, the voltage coupling circuit includes a first capacitor coupled to the first terminal of the voltage coupling circuit and the gate terminal of the first transistor, and a second capacitor coupled to the first terminal of the voltage coupling circuit and the gate terminal of the second transistor.

[009] In yet another aspect, the voltage coupling circuit further includes a clamping circuit, a first resistor and a second resistor, the clamping circuit coupled to

the first resistor and the gate terminal of the first transistor, and the first resistor coupled to the clamping circuit and the cathode of the rectifier, and the second resistor coupled to the gate terminal of the second transistor and the cathode of the rectifier.

[010] In still another aspect, the clamping circuit clamps the first voltage signal provided to the gate terminal of the first transistor, and the first and second resistors, in conjunction with the first and second capacitors, control a time delay to turn on the rectifier.

[011] Also in accordance with the present invention, there is provided an integrated circuit that includes a signal pad for receiving and outputting a signal, a rectifier with an anode and a cathode including a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, and a second n-type portion contiguous with the second p-type portion, wherein the anode of the rectifier is coupled to the signal pad, a first transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the first n-type portion of the rectifier, and a second transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the second n-type portion of the rectifier, and the second terminal is coupled to the second terminal of the first transistor.

[012] In one aspect, the circuit further comprises an output buffer having a first terminal and a second terminal, wherein the first terminal is coupled to the signal pad and the second terminal is coupled to the first capacitor and the second capacitor.

[013] Additionally in accordance with the present invention, there is provided an integrated circuit that includes an output buffer having a first terminal and a second terminal, a rectifier with an anode and a cathode including a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, and a second n-type portion contiguous with the second p-type portion, wherein the anode of the rectifier is coupled to the first terminal of the output buffer, a first transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the first n-type portion of the rectifier, and a second transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the second –type portion of the rectifier, and the second terminal is coupled to the second terminal of the first transistor.

[014] Also in accordance with the present invention, there is provided an integrated circuit that includes a signal pad for receiving and outputting a signal, an output buffer having a first terminal and a second terminal, wherein the second terminal is coupled to the signal pad, a rectifier, having an anode and a cathode, including a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, and a second n-type portion contiguous with the second p-type portion, wherein the first p-type portion is coupled to the anode, the second n-type portion is coupled to the cathode, the anode is coupled to the first terminal of the output buffer, and the cathode is coupled to ground, a first transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the first n-type

portion of the rectifier, a second transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the second terminal of the first transistor, and the second terminal is coupled to the second n-type portion of the rectifier, and a voltage coupling circuit having a first terminal, a second terminal, a third terminal and a fourth terminal, wherein the first terminal is coupled to the anode of the rectifier, the second and the third terminals are respectively coupled to the gate terminals of the first and second transistor, and the fourth terminal is coupled to the cathode of the rectifier.

[015] Additionally in accordance with the present invention, there is provided an integrated circuit that includes a signal pad for receiving and outputting a signal, an output buffer having a first terminal and a second terminal, wherein the second terminal is coupled to the signal pad, a rectifier with an anode and a cathode including a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, and a second n-type portion contiguous with the second p-type portion, wherein the anode of the rectifier is coupled to the second terminal of the output buffer and the cathode of the rectifier is coupled to ground, a first transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the first n-type portion of the rectifier, a second transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the second terminal of the first transistor, and the second terminal is coupled to the second n-type portion of the rectifier; and a voltage coupling circuit having a first terminal, a second terminal, a third terminal and a fourth terminal, wherein the first terminal is coupled to the first

terminal of the output buffer, the second and the third terminals are respectively coupled to the gate terminals of the first and second transistor, and the fourth terminal is coupled to the cathode of the rectifier.

[016] Further in accordance with the present invention, there is provided a method for protecting an integrated circuit with a dual input/output pad from electrostatic discharge that includes providing a rectifier having a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, and a second n-type portion contiguous with the second p-type portion, providing a first transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the first n-type portion of the rectifier, and providing a second transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the second n-type portion of the rectifier, and the second terminal is coupled to the second terminal of the first transistor.

[017] In one aspect, the method further includes a step of providing a first voltage signal to the gate of the first transistor and a second voltage signal to the gate of the second transistor to turn on the rectifier.

[018] Additional objects and advantages of the invention will be set forth in part in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention will be realized and attained by means of the elements and combinations particularly pointed out in the appended claims.

[019] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

[020] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate several embodiments of the invention and together with the description, serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[021] Fig. 1 is a circuit diagram of a known ESD protection circuit;

[022] Fig. 2 is a circuit diagram in accordance with one embodiment of the present invention;

[023] Fig. 3 is a circuit diagram in accordance with the embodiment shown in Fig. 2 with the SNTSCR device shown in a cross-sectional view;

[024] Fig. 4 is a circuit diagram in accordance with another embodiment of the present invention;

[025] Fig. 5 is an alternate representation of the embodiment shown in Fig. 2;

[026] Fig. 6 is a circuit diagram in accordance with another embodiment of the present invention; and

[027] Fig. 7 is a circuit diagram in accordance with another embodiment of the present invention.

DESCRIPTION OF THE EMBODIMENTS

[028] Reference will now be made in detail to the present exemplary embodiments of the invention, examples of which are illustrated in the

accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[029] In accordance with the present invention, there is provided a stacked-NMOS transistor-triggered silicon controlled rectifier ESD protection circuit. ESD protection is achieved with a gate-coupling technique in a stacked-NMOS transistor-triggered silicon controlled rectifier ("SNTSCR") ESD protection device implemented in an I/O buffer. The ESD protection device of the present invention has a low trigger voltage to protect thin oxide layers in mixed-voltage sub-micron CMOS ICs. The SNTSCR of the present invention ensures the reliability and safety of an I/O buffer in a mixed voltage environment, and provides higher ESD robustness with a smaller layout area.

[030] Fig. 2 is a circuit diagram of one embodiment of the present invention. Referring to Fig. 2, an integrated circuit ("IC") 10 includes an I/O pad 24, I/O buffer 28, ESD clamp circuit 22, and an internal circuit 26. I/O buffer 28 includes a transistor 30 and stacked transistors 32 and 34, in which the source terminal (not numbered) of transistor 32 is coupled to the drain terminal (not numbered) of transistor 34. The gate terminal of transistor 32 is coupled to a voltage source VDD. The gate terminal of transistor 34 is coupled to internal circuit 26, and the source terminal is coupled to VSS, or ground. In one embodiment, transistor 30 is a PMOS transistor with a floating n-well, and transistors 32 and 34 are NMOS transistors. Transistor 30 has a source terminal 30-3, gate terminal 30-4, drain terminal 30-2, and n-well terminal 30-1. Source terminal 30-3 is coupled to voltage source VDD,

gate terminal 30-4 is coupled to internal circuit 26, and drain terminal 30-2 is coupled to I/O pad 24 and the drain of transistor 32.

[031] ESD clamp circuit 22 includes a parasitic silicon controlled rectifier ("SCR") 12, stacked transistors 36 and 38, a voltage coupling circuit (not numbered). SCR 12 includes a first p-type portion 14, a first n-type portion 16 contiguous with first p-type portion 14, a second p-type portion 18 contiguous with first n-type portion 16, and a second n-type portion 20 contiguous with second p-type portion 18. First p-type portion 14 is coupled to an anode terminal (not shown) and second n-type portion 20 is coupled to a cathode terminal (not shown). In addition, the cathode terminal of SCR 12 is coupled to VSS, or ground, and the anode terminal is coupled to I/O pad 24.

[032] Transistor 36 include a drain terminal 36-1, gate terminal 36-2, and source terminal 36-3. Transistor 38 includes a drain terminal 38-1, gate terminal 38-2, and source terminal 38-3. In one embodiment, transistors 36 and 38 are NMOS transistors. Source terminal 36-3 of transistor 36 is coupled to drain terminal 38-1 of transistor 38, and drain terminal 36-1 of transistor 36 is coupled to first n-type portion 16 of SCR 12. Source terminal 38-3 is coupled to second n-type portion 20 of SCR 12. Gate terminals 36-2 and 38-2 are coupled to the voltage coupling circuit.

[033] The voltage coupling circuit includes a first capacitor 42, a second capacitor 44, a transistor 50, a resistor network (not numbered), and a clamping circuit (not numbered). First capacitor 42 is coupled to gate terminal 36-2 of transistor 36, and second capacitor 44 is coupled to gate terminal 38-2 of transistor 38. First capacitor 42 and second capacitor 44 are also coupled in parallel to I/O

pad 24. Transistor 50 is a diode-connected NMOS transistor. The drain terminal (not numbered) of transistor 50 is coupled to a voltage source, VDD, and the gate (not numbered) of transistor 50. The source of transistor 50 is coupled to gate terminal 36-2 of transistor 36 and first capacitor 42.

[034] The resistor network includes a first resistor 46 and a second resistor 40. First resistor 46 is coupled to second capacitor 44 and gate terminal 38-2 of transistor 38. Each of first resistor 46 and second resistor 40 is coupled to VSS. The clamping circuit of the ESD clamp circuit 22 includes a transistor 48. In one embodiment, transistor 48 is a PMOS transistor. The gate (not numbered) of transistor 48 is coupled to voltage source VDD, and the source (not numbered) of transistor 48 is coupled to gate terminal 36-2 of transistor 36 and the source of transistor 50. The drain (not numbered) of transistor 48 is coupled to resistor 40.

[035] Fig. 3 shows a circuit diagram in accordance with the embodiment shown in Fig. 2 with SCR device 12 shown in a cross-sectional view. Referring to Fig. 3, second p-type portion 18 of SCR 12 comprises a p-type semiconductor substrate 18. First n-type portion 16 comprises an n-well 16 formed inside substrate 18. First p-type portion 14 comprises a p-type diffused region 14 formed inside N-well 16. Second n-type portion 20 comprises an n-type diffused region 20 formed inside substrate 18 and an n-well 52, and is spaced apart from first n-type portion 16. A path 60 indicates the path of an ESD current in SCR 12 when SCR 12 is triggered by an ESD event.

[036] Substrate 18 also includes a p-type diffused region 56, and a shallow trench isolation ("STI") 54 contiguous with p-type diffused region 56, n-well 52 and n-

type diffused region 20. Each of p-type diffused region 56 and n-type diffused region 20 is coupled to ground. In addition, stacked transistors 36 and 38 are formed on substrate 18. Transistor 36 includes a gate 36-2, drain 36-1 and source 62. Transistor 38 includes a gate 38-2, drain 62, and source 20. Therefore, drain 36-1 of transistor 36 comprises diffused n-type region 36-1 formed contiguous with n-well 16 and inside substrate 18. Source 36-3 of transistor 36 and drain 38-1 of transistor 38 share the same diffused n-type region 62 formed inside substrate 18.

[037] Referring to Fig. 2, in operation, ESD clamp circuit 22 should remain in a non-conductive state so that it does not interfere with the voltages levels on I/O pad 24 during normal operations. The voltage on gate terminal 36-2 of transistor 36 is biased at VDD-Vthn through the diode-connected NMOS transistor 50, wherein Vthn is the threshold voltage of transistor 50. Gate terminal 38-2 of transistor 38 is coupled to ground. Under these conditions, diffused n-type region 62, shared by stacked transistors 36 and 38, floats to a voltage of approximately one threshold voltage below VDD. Therefore, the ESD clamp circuit 22 is able to meet the limited stress constraints of a gate oxide during normal operating conditions.

[038] Referring again to Fig. 2, I/O pad 24 may either receive or output a signal. As an input pad, I/O pad 24 receives a logic "0" signal and a logic "1" signal. I/O pad 24 then couples the signal to I/O buffer 28. As the voltage on I/O pad 24 transfers from a logic "0" to a logic "1," capacitor 44 functions to couple a voltage below the threshold voltage to gate terminal 38-2 of transistor 38 to keep transistor 38 in the "off" state, thereby keeping SCR 12 in the "off" state. ESD Clamp circuit 22, which comprises transistor 48, will then turn on to discharge any excessive

charge after the gate voltage of transistor 36 increases to VDD+Vthp, wherein Vthp is the threshold voltage of transistor 48. Therefore, clamping circuit 22 clamps the voltage of gate terminal 36-2 to ensure the reliability of the gate oxide under normal operating conditions.

[039] When a positive-to-VSS ESD signal is provided to I/O pad 24, the voltage coupling circuit provides a first voltage signal to transistor 36 and a second voltage signal to transistor 38 to turn on SCR 12 to divert the ESD signal away from internal circuit 26. The resistor network is provided to control a time delay in the triggering of SCR 12.

[040] Fig. 5 is an alternate representation of the embodiment shown in Fig. 2 and is used to illustrate the ESD current path under four modes of ESD-stresses. In an ESD event with a large positive input voltage with respect to VSS, ESD clamp circuit 22 works to shunt the ESD current to ground. In an ESD event with a large positive input voltage with respect to VDD, a parasitic diode 66, formed by p-type substrate 18 and n-well 16 (shown in Fig. 3), turns on. The ESD current flows through the SCR 12 and parasitic diode 66 to VDD. In an ESD event with a large negative input voltage with respect to VSS, a parasitic diode 64, formed by p-type substrate 18 and diffused n-type region 20 (shown in Fig. 3), turns on to bypass the ESD current. In an ESD event with a large negative input voltage with respect to VDD, the ESD current flows through a rail clamp circuit 68 and parasitic diode 64 to shunt the ESD current.

[041] Fig. 4 shows a circuit diagram in accordance with another embodiment of the present invention. Referring to Fig. 4, an integrated circuit 10

includes an I/O pad 24, I/O buffer 28, ESD clamp circuit 22, and an internal circuit 26. I/O buffer 28 includes a transistor 30 and stacked transistors 32 and 34, in which the source terminal (not numbered) of transistor 32 is coupled to the drain terminal (not numbered) of transistor 34. The gate terminal of transistor 32 is coupled to a voltage source VDD. The gate terminal of transistor 34 is coupled to internal circuit 26, and the source terminal is coupled to VSS, or ground. In one embodiment, transistor 30 is a PMOS transistor, and transistors 32 and 34 are NMOS transistors. Transistor 30 has a source terminal 30-3, gate terminal 30-4, drain terminal 30-2, and an n-well 30-1. Source terminal 30-3 is coupled to voltage source VDD, gate terminal 30-4 is coupled to internal circuit 26, and drain terminal 30-2 is coupled to I/O pad 24 and the drain of transistor 32.

[042] ESD clamp circuit 22 includes a (SCR) 12, two stacked transistors 36 and 38, a voltage coupling circuit (not numbered). SCR 12 includes a first p-type portion 14, a first n-type portion 16 contiguous with first p-type portion 14, a second p-type portion 18 contiguous with first n-type portion 16, and a second n-type portion 20 contiguous with second p-type portion 18. First p-type portion 14 is coupled to an anode terminal (not shown) and second n-type portion 20 is coupled to a cathode terminal (not shown). In addition, the cathode terminal of SCR 12 is coupled to VSS and the anode terminal is coupled to n-well 30-1 of transistor 30. In other words, I/O buffer 28 includes a first terminal (not numbered) coupled to I/O pad 24 and a second terminal 30-1 coupled to ESD clamp circuit 22.

[043] Transistor 36 include a drain terminal 36-1, gate terminal 38-2, and source terminal 38-3. Transistor 38 includes a drain terminal 38-1, gate terminal 36-

2, and source terminal 36-3. In one embodiment, transistors 36 and 38 are NMOS transistors. Source terminal 36-3 of transistor 36 is coupled to drain terminal 38-1 of transistor 38, and drain terminal 36-1 of transistor 36 is coupled to first n-type portion 16 of SCR 12. Source terminal 38-3 is coupled to second n-type portion 20 of SCR 12. Gate terminals 36-2 and 38-2 are coupled to the voltage coupling circuit.

[044] The voltage coupling circuit includes a first capacitor 42, a second capacitor 44, a transistor 50, a resistor network (not numbered), and a clamping circuit (not numbered). First capacitor 42 is coupled to gate terminal 36-2 of transistor 36, and second capacitor 44 is coupled to gate terminal 38-2 of transistor 38. First capacitor 42 and second capacitor 44 are also coupled in parallel to n-well 30-1 of transistor 30 and the anode of SCR 12. Transistor 50 is a diode-connected NMOS transistor. The drain terminal (not numbered) of transistor 50 is coupled to a voltage source, VDD, and the gate (not numbered) of transistor 50. The source of transistor 50 is coupled to gate terminal 36-2 of transistor 36 and first capacitor 42.

[045] The resistor network includes a first resistor 46 and a second resistor 40. First resistor 46 is coupled to second capacitor 44 and gate terminal 38-2 of transistor 38. Each of first resistor 46 and second resistor 40 is coupled to VSS. The clamping circuit of the ESD clamp circuit 22 includes a transistor 48. In one embodiment, transistor 48 is a PMOS transistor. The gate (not numbered) of transistor 48 is coupled to voltage source VDD, and the source (not numbered) of transistor 48 is coupled to gate terminal 36-2 of transistor 36 and the source of transistor 50. The drain (not numbered) of transistor 48 is coupled to resistor 40.

[046] The primary difference of Fig. 4 from Fig. 2 is that capacitors 42 and 44, and the anode terminal of SCR 12 are coupled to n-well terminal 30-1 of transistor 30. This embodiment provides a clamping configuration to ensure that no additional input capacitance is seen at I/O pad 24, an important factor in high-frequency applications.

[047] Fig. 6 is a circuit diagram in accordance with another embodiment of the present invention. Figs. 4 and 6 are essentially the same with the difference being the connecting between I/O buffer 28 and ESD clamp circuit 22. Specifically, terminal 30-1, also the n-well of transistor 30, of I/O buffer 28 is coupled to parallel capacitors 42 and 44 of ESD clamp circuit 22. The anode of SCR 12 of ESD clamp circuit 22 is coupled to I/O pad 24 and drain 30-2 of transistor 30. ESD clamp circuit 22 is connected from n-well terminal 30-1 of PMOS transistor 30, wherein the parasitic drain-to-substrate diode between I/O pad 24 and n-well terminal 30-1 essentially exists in PMOS transistor 30. Only noise having a level higher than the voltage level of n-well terminal 30-1 plus a voltage drop across a diode can reach ESD clamp circuit 22.

[048] The present invention also discloses a method to protect an IC in mixed-voltage applications from an ESD event. The method includes providing a parasitic rectifier having a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, and a second n-type portion contiguous with the second p-type portion and providing a first transistor having a first terminal, a second terminal and a gate terminal. The first terminal of the first transistor is coupled to the first n-type portion

of the rectifier. The method also includes providing a second transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the second n-type portion of the rectifier, and the second terminal is coupled to the second terminal of the first transistor. The method further includes providing a first voltage signal to the gate of the first transistor and a second voltage signal to the gate of the second transistor to turn on the rectifier.

[049] Fig. 7 is a circuit diagram in accordance with another embodiment of the present invention. Figs. 2 and 7 are similar except for a gate coupling circuit that comprises NMOS transistor 58. Referring to Fig. 7, the gate coupling circuit is added in ESD clamp circuit 22 to improve the design margin. Transistor 58 is disposed between gate terminal 38-2 of transistor 38 and VSS, and the gate terminal of transistor 58 is coupled to VDD. As a result, under normal operating conditions, transistor 58 is always turned on, thereby reducing the coupling voltage on gate terminal 38-2 of transistor 38 below the threshold voltage of transistor 38 to avoid any unexpected leakage current. During an ESD event, transistor 58 is off once the initial voltage level on the floating VDD power line is grounded, and the coupling voltage on the gate terminal 38-2 is determined by the first resistor 46 and the second capacitor 44.

[050] Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.